XS5A1T4157-Q100

Low-ohmic single-pole double-throw analog switch

Rev. 1 — 8 November 2023 Product data sheet

1. General description

The XS5A1T4157-Q100 is a low-ohmic single-pole double-throw analog switch suitable for use as an analog or digital 2:1 multiplexer/demultiplexer. It has a digital select input (S), two inputs/outputs (Y0 and Y1) and a common input/output (Z).

The XS5A1T4157-Q100 passes analog and digital voltages that may vary across the full voltage supply range (GND to V_{CC}).

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
  - Specified from -40 °C to +85 °C and from -40 °C to +125 °C
- Supply voltage range from V_{CC} = 4.5 V to 5.5 V
- Very low ON resistance: 4 Ω (typical) at V_{CC} = 5 V
- Switch inputs voltage range: V_{SW} = GND to V_{CC}
- Control input voltage range: $V_{I(S)}$ = GND to V_{CC}
- Latch-up performance exceeds 200 mA per JESD 78 Class II level A
- ESD protection:
  - HBM: ANSI/ESDA/Jedec JS-001 Class 2 exceeds 2 kV
  - CDM: ANSI/ESDA/Jedec JS-002 Class C3 exceeds 1 kV

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
XS5A1T4157GW-Q100	-40 °C to +125 °C	TSSOP6	plastic thin shrink small outline package; 6 leads; body width 1.25 mm	SOT363-2

4. Marking

Table 2. Marking codes

Type number	Marking code[1]
XS5A1T4157GW-Q100	zb

[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

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5. Functional diagram

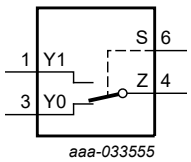
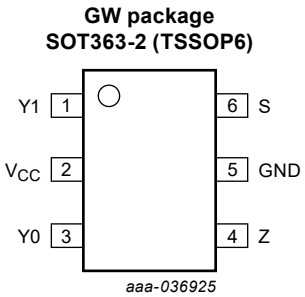


Fig. 1. Logic symbol

6. Pinning information

6.1. Pinning



6.2. Pin description

Table 3. Pin description

Symbol	Pin	Description
Y1	1	independent input or output
V_{CC}	2	supply voltage
Y0	3	independent input or output
Z	4	common output or input
GND	5	ground (0 V)
S	6	select input

7. Functional description

Table 4. Function table

H = HIGH voltage level; L = LOW voltage level.

Input	Channel on
S	
L	Y0
H	Y1

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+6.5	V
V_I	input voltage	S input [1]	-0.5	+6.5	V
I_{IK}	input clamping current	S input; V_I < -0.5 V	-50	-	mA
I_{SK}	switch clamping current	Z, Y0 and Y1 inputs/outputs; V_{SW} < -0.5 V or V_{SW} > V_{CC} + 0.5 V	-	±50	mA
V_{SW}	switch voltage	Z, Y0 and Y1 inputs/outputs [2]	- 0.5	V_{CC} + 0.5	V
I_{SW}	switch current	Z, Y0 and Y1 inputs/outputs; [3] -0.5 V < V_{SW} < V_{CC} + 0.5 V	-	±128	mA
$T_{j(max)}$	maximum junction temperature		-	+150	°C
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	T_{amb} = -40 °C to +125 °C [4]	-	250	mW

[1] The minimum input voltage rating may be exceeded if the input current rating is observed.
[2] The minimum and maximum switch voltage ratings may be exceeded if the switch clamping current rating is observed.
[3] Continuous current sustained maximum of 2 years.
[4] For SOT363-2 (TSSOP6) package: P_{tot} derates linearly with 3.7 mW/K above 83 °C.

9. Recommended operating conditions

Table 6. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		4.5	5.5	V
V_I	input voltage	S input	0	5.5	V
V_{SW}	switch voltage	Z, Y0 and Y1 inputs/outputs	0	V_{CC}	V
I_{SW}	switch current	Z, Y0 and Y1 inputs/outputs; -0.5 V < V_{SW} < V_{CC} + 0.5 V	-	±64	mA
T_{amb}	ambient temperature		-40	+125	°C
Δt/ΔV	input transition rise and fall rate	S input	-	100	ns/V

10. Static characteristics

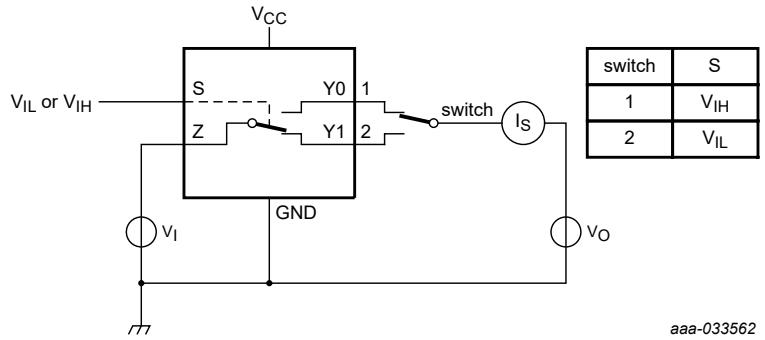
Table 7. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground 0 V).

Symbol	Parameter	Conditions	T_{amb} = -40 °C to +125 °C			Unit
			Min	Typ[1]	Max	
V_{IH}	HIGH-level input voltage	S input; V_{CC} = 4.5 V to 5.5 V	1.4	-	-	V
V_{IL}	LOW-level input voltage	S input; V_{CC} = 4.5 V to 5.5 V	-	-	0.3	V
I_I	input leakage current	S input; $V_{I(S)}$ = 5.5 V	-50	0.2	50	nA
$I_{S(OFF)}$	OFF-state leakage current	$V_{I(S)}$ = V_{IL} or V_{IH}; V_I = 1.5 V or 4.5 V; V_O = 4.5 V or 1.5 V; V_{CC} = 5.0 V; see Fig. 2	-320	±0.02	320	nA
$I_{S(ON)}$	ON-state leakage current	$V_{I(S)}$ = V_{IL} or V_{IH}; V_I = V_O = 1 V or 4.5 V; V_{CC} = 5.0 V; see Fig. 3	-320	±0.02	320	nA
I_{CC}	supply current	$V_{I(S)}$ = GND or V_{CC}; V_{SW} = GND or V_{CC}; V_{CC} = 5.0 V	-	0.6	8000	nA
		$V_{I(S)}$ = 1.8 V; V_{SW} = GND or V_{CC}; V_{CC} = 5.0 V; see Fig. 4	-	90	-	µA
C_I	input capacitance	S input; V_{CC} = 5.0 V	-	2	-	pF
$C_{S(OFF)}$	OFF-state capacitance	Y0, Y1 input/output; V_{CC} = 5.0 V; see Fig. 5	-	11	-	pF
$C_{S(ON)}$	ON-state capacitance	Z input/output; V_{CC} = 5.0 V; see Fig. 6	-	35	-	pF

[1] Typical values are measured at T_{amb} = 25 °C.

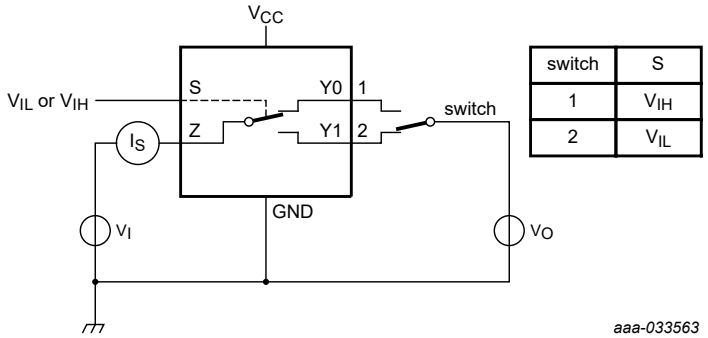
10.1. Test circuits and graphs



switch	S
1	V_{IH}
2	V_{IL}

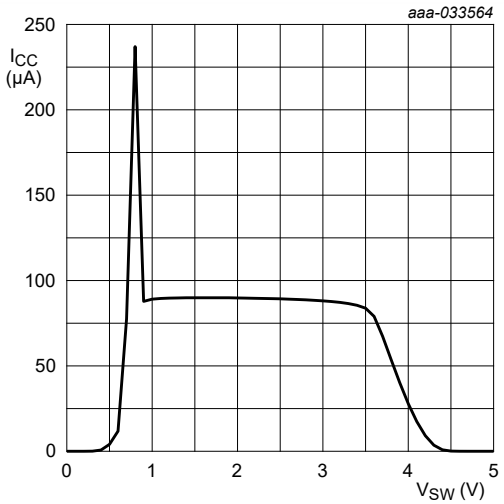
V_I = 1.5 V or 4.5 V; V_O = 4.5 V or 1.5 V

Fig. 2. Test circuit for measuring OFF-state leakage current



$V_I = V_O$ = 1 V or 4.5 V

Fig. 3. Test circuit for measuring ON-state leakage current



T_{amb} = 25 °C; V_{CC} = 5.0 V

Fig. 4. Typical supply current as function of the switch voltage

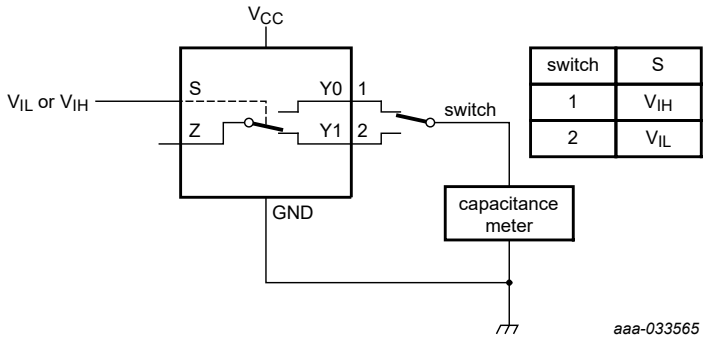


Fig. 5. Test circuit for measuring OFF-state capacitance

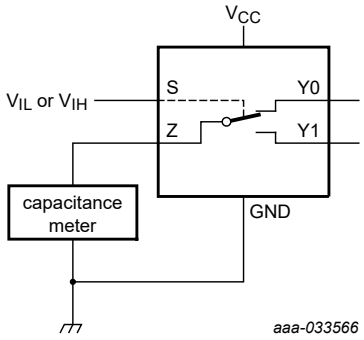


Fig. 6. Test circuit for measuring ON-state capacitance

10.2. ON resistance

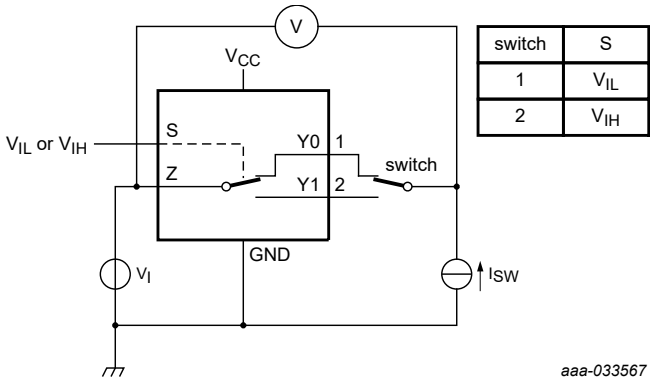
Table 8. ON resistance

At recommended operating conditions; voltages are referenced to GND (ground 0 V);
For test circuit see Fig. 7; for graphs see Fig. 8 and Fig. 9.

Symbol	Parameter	Conditions	T_{amb} = -40 °C to +125 °C			Unit
			Min	Typ[1]	Max	
$R_{ON(peak)}$	ON resistance (peak)	$V_{I(S)}$ = V_{IL} or V_{IH}; $V_{I(Z)}$ = GND to V_{CC}; V_{CC} = 4.5 V to 5.5 V [2]				
		I_{SW} = 10 mA	2.2	4.0	7.5	Ω
		I_{SW} = 32 mA	2.2	4.0	7.7	Ω
		I_{SW} = 64 mA	2.2	4.0	7.7	Ω
ΔR_{ON}	ON resistance mismatch between channels	I_{SW} = 64 mA; $V_{I(Z)}$ = GND to V_{CC}; V_{CC} = 4.5 V to 5.0 V [2]	-	90	-	mΩ
$R_{ON(flat)}$	ON resistance (flatness)	$V_{I(S)}$ = V_{IL} or V_{IH}; $V_{I(Z)}$ = GND to V_{CC}; V_{CC} = 4.5 V to 5.0 V [2] [3]				
		I_{SW} = 10 mA	0.2	0.8	3	Ω
		I_{SW} = 32 mA	0.2	0.8	3	Ω
		I_{SW} = 64 mA	0.2	0.9	3	Ω

[1] Typical values are measured at T_{amb} = 25 °C.
[2] Measured by the voltage drop between Z and Yn pins at the indicated current through the switch. ON resistance is determined by the lower of the voltages on the two (Z or Yn pins).
[3] Flatness is defined as the difference between the maximum and minimum value of ON resistance over the specified range of conditions.

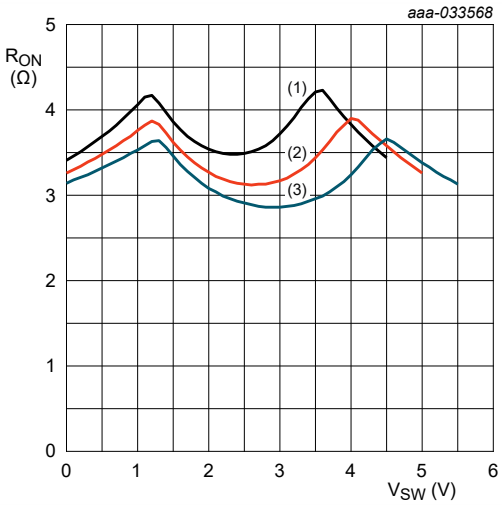
10.3. ON resistance test circuit and graphs



switch	S
1	V_{IL}
2	V_{IH}

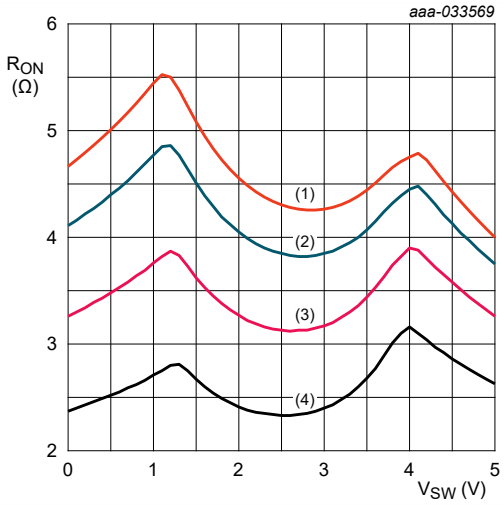
$R_{ON} = V / I_{SW}$

Fig. 7. Test circuit for measuring ON resistance



I_{SW} = 10 mA
(1) V_{CC} = 4.5 V
(2) V_{CC} = 5.0 V
(3) V_{CC} = 5.5 V

Fig. 8. Typical ON resistance as a function of input voltage; T_{amb} = 25 °C



I_{SW} = 10 mA
(1) T_{amb} = 125 °C
(2) T_{amb} = 85 °C
(3) T_{amb} = 25 °C
(4) T_{amb} = -40 °C

Fig. 9. ON resistance as a function of input voltage; V_{CC} = 5.0 V

11. Dynamic characteristics

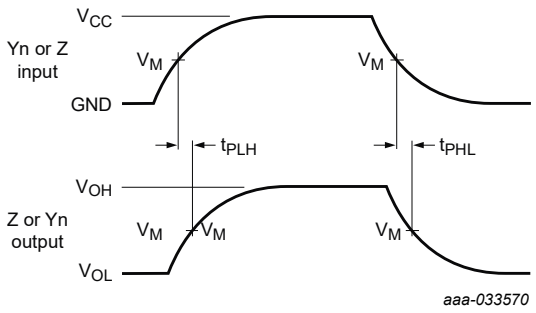
Table 9. Dynamic characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	T_{amb} = -40 °C to +125 °C			Unit
			Min	Typ[1]	Max	
t_{pd}	propagation delay	Z to Yn or Yn to Z; see Fig. 10 and Fig. 12; [2] V_{CC} = 4.5 V to 5.5 V	-	0.4	1.0	ns
t_{TRAN}	transition time between channels	S to Z or Yn; see Fig. 11 and Fig. 13; V_{CC} = 4.5 V to 5.5 V	10	23	40	ns
t_{b-m}	break-before-make time	C_L = 15 pF; R_L = 200 Ω; see Fig. 14; V_{CC} = 4.5 V to 5.5 V	1	7.5	17	ns

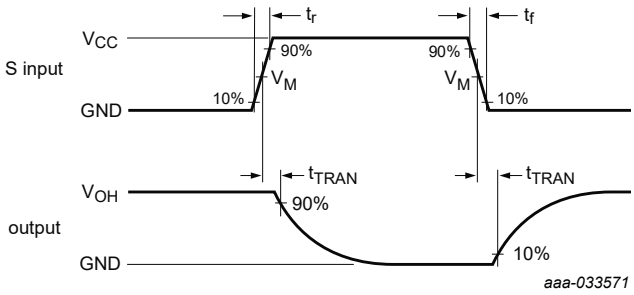
[1] Typical values are measured at T_{amb} = 25 °C.
[2] t_{pd} is the same as t_{PLH} and t_{PHL}

11.1. Waveforms and test circuits



Measurement points are given in Table 10.
Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.
Rise and fall times strongly depend on source impedance and load capacitance.

Fig. 10. Input (Yn or Z) to output (Z or Yn) propagation delays

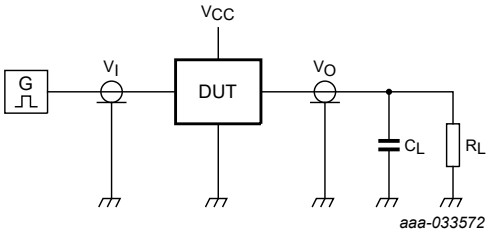


Measurement points are given in Table 10.
Logic levels: V_{OH} is a typical output voltage level that occur with the output load.

Fig. 11. Transition time between channels

Table 10. Measurement points

Supply voltage	Input	Output
V_{CC}	V_M	V_M
GND to V_{CC}	50%	50%



Test data is given in Table 11.

All input pulses are supplied by generators having the following characteristics:

PRR ≤ 10 MHz; Z_O = 50 Ω; t_r, t_f =2 ns.

Definitions test circuit:

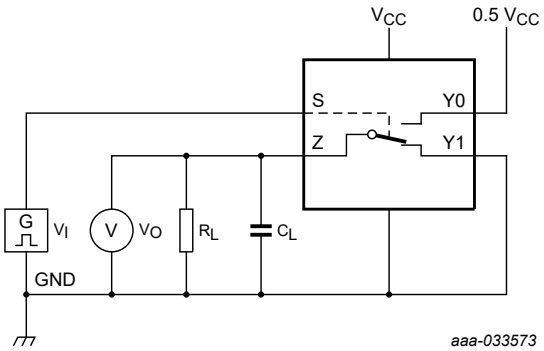
C_L = Load capacitance (including jig and probe capacitance).

R_L = Load resistance.

Fig. 12. Test circuit for measuring propagation delay times

Table 11. Test data

Load	
C_L	**R_L**
100 pF	1 MΩ



Test data is given in Table 12.

All input pulses are supplied by generators having the following characteristics:

PRR ≤ 10 MHz; Z_O = 50 Ω.

Definitions test circuit:

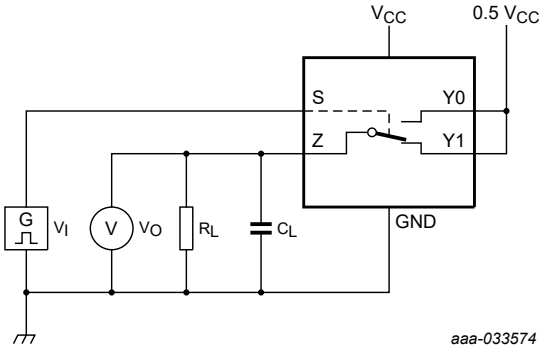
C_L = Load capacitance (including jig and probe capacitance).

R_L = Load resistance.

Fig. 13. Test circuit for measuring transition times between channels

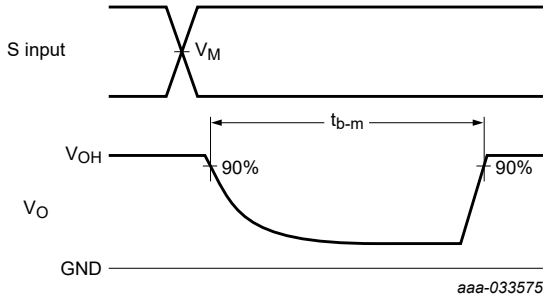
Table 12. Test data

Input S	**Load**	
t_r, t_f	**C_L**	**R_L**
≤ 2 ns	15 pF	1 MΩ



a. Test circuit

All input pulses are supplied by generators having the following characteristics:
PRR ≤ 10 MHz; Z_O = 50 Ω; t_r, t_f = 2 ns.



b. Input and output measurement points

Fig. 14. Test circuit for measuring break-before-make times

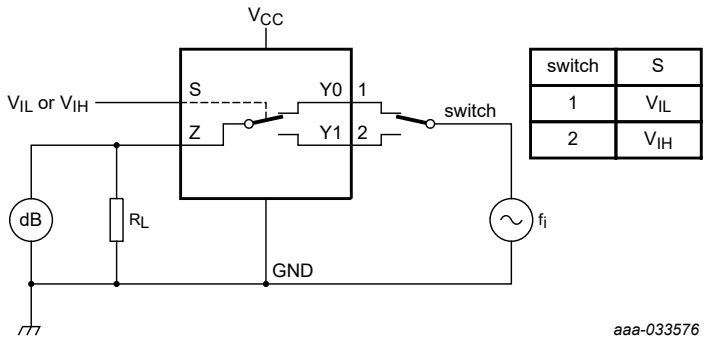
11.2. Additional dynamic characteristics

Table 13. Additional dynamic characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	T_{amb} = 25 °C			
			Min	Typ	Max	Unit
$f_{(-3dB)}$	-3 dB frequency response	R_L = 50 Ω; see Fig. 15; V_{CC} = 5.0 V	-	190	-	MHz
α_{iso}	isolation (OFF-state)	R_L = 50 Ω; f_i = 10 MHz; see Fig. 16; V_{CC} = 5.0 V	-	-56	-	dB
Xtalk	crosstalk	between switches; R_L = 50 Ω; f_i = 1 MHz; V_{CC} = 5.0 V; see Fig. 17	-	-76	-	dB
Q_{inj}	charge injection	C_L = 1 nF; V_{gen} = 0.5V_{CC}; R_{gen} = 0 Ω; f_i = 1 MHz; R_L = 1 MΩ; V_{CC} = 5.0 V; see Fig. 18	-	4.5	-	pC

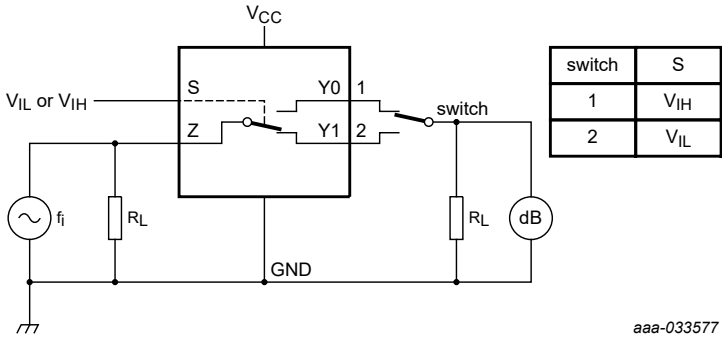
11.3. Test circuits



switch	S
1	V_{IL}
2	V_{IH}

f_i voltage source: Z_O = 50 Ω. The f_i voltage level is set for R_L = 50 Ω: DC = 0.5V_{CC}, AC = 0 dBm. Increase f_i frequency until dB meter reads -3 dB

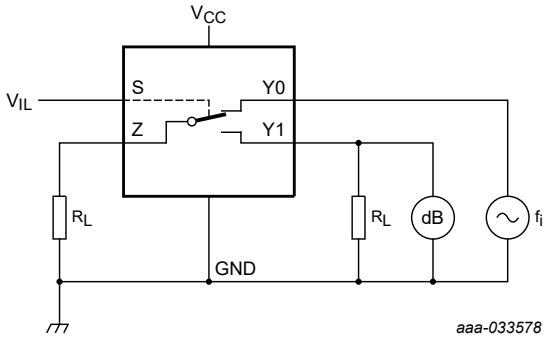
Fig. 15. Test circuit for measuring the -3 dB frequency response when switch is in ON-state



switch	S
1	V_{IH}
2	V_{IL}

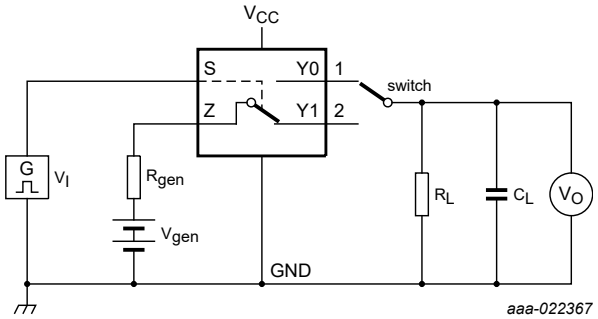
f_i voltage source: Z_O = 50 Ω. The f_i voltage level is set for R_L = 50 Ω: DC = 0.5V_{CC}, AC = 0 dBm.

Fig. 16. Test circuit for measuring isolation (OFF-state)

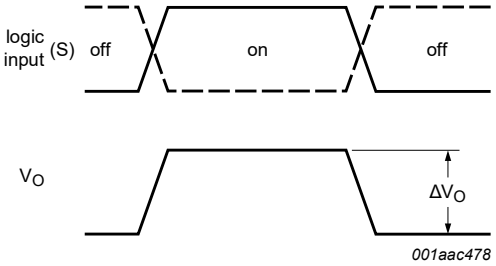


f_i voltage source: Z_O = 50 Ω. The f_i voltage level is set for R_L = 50 Ω: DC = 0.5V_{CC}, AC = 0 dBm.

Fig. 17. Test circuit for measuring crosstalk between switches



a. Test circuit



b. Input and output pulse definitions

Definitions for test circuit:

$Q_{inj} = \Delta V_O \times C_L$;

ΔV_O = output voltage variation;

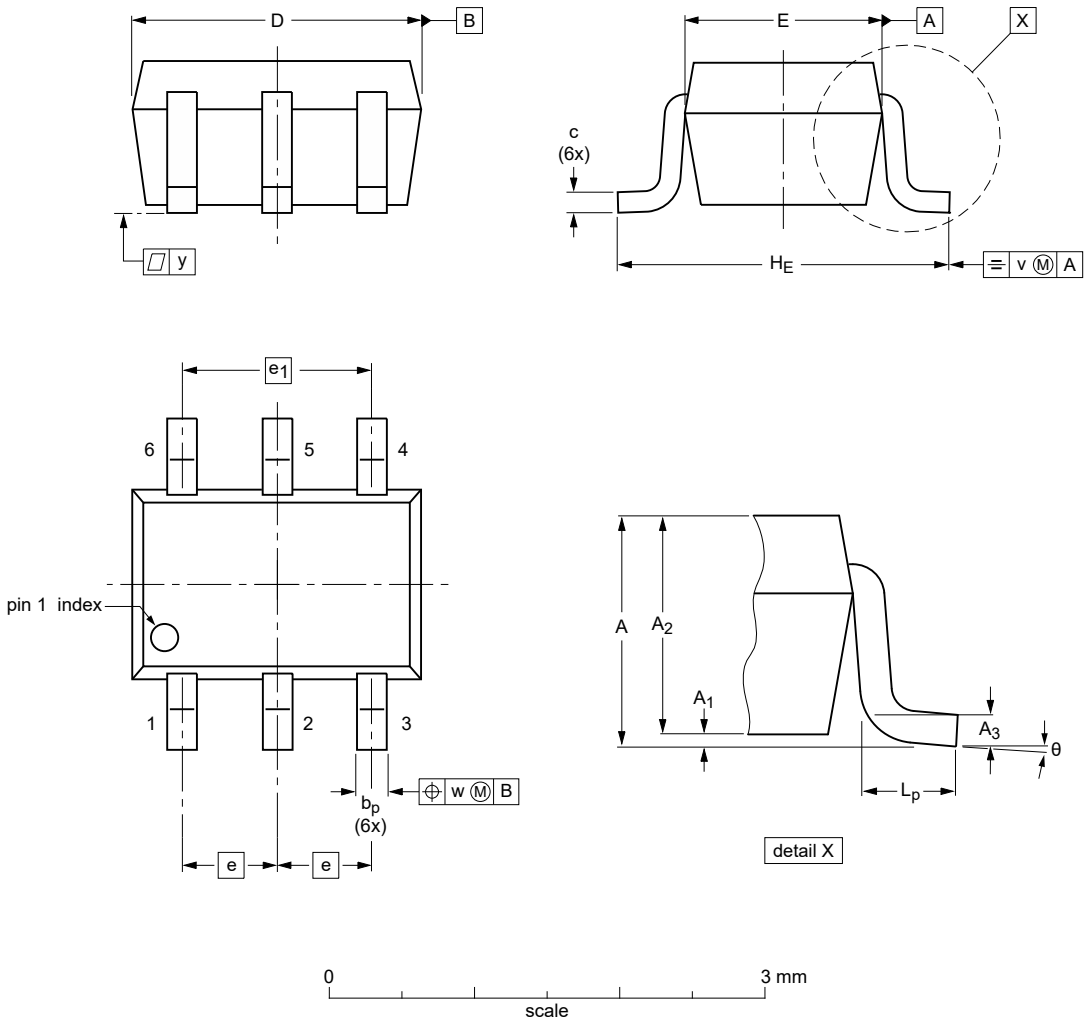
R_{gen} = generator resistance;

V_{gen} = generator voltage.

Fig. 18. Test circuit for measuring charge injection

12. Package outline

TSSOP6: plastic thin shrink small outline package; 6 leads; body width 1.25 mm **SOT363-2**



Dimensions (mm are the original dimensions)

Unit		A	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	e_1	H_E	L_p	v	w	y	θ
mm	max	1.1	0.1	1.0	0.15	0.30	0.25	2.2	1.35	0.65	1.3	2.4	0.46	0.3	0.1	0.1	8°
	min	0.8	0	0.8		0.15	0.08	1.8	1.15			1.8	0.26				0°

Note

1. Plastic or metal protrusions of 0.2 mm maximum per side are not included.

sot363-2_po

Outline version	References			European projection	Issue date
	IEC	JEDEC	JEITA		
SOT363-2		MO-203	SC-88A		~~21-12-15~~ 21-12-16

Fig. 19. Package outline SOT363-2 (TSSOP6)

13. Abbreviations

Table 14. Abbreviations

Acronym	Description
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
PRR	Pulse Rate Repetition

14. Revision history

Table 15. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
XS5A1T4157_Q100 v.1	20231108	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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